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QUARTERLY REPORT NO. 7
FOR
ANALOG-TO-DIGITAL CONVERTER
CONTRACT NO. N00014-87-C-0314
1 OCTOBER 1988 - 31 DECEMBER 1988

ARPA Order Number:	9117
Program Code Number:	7220
Amount of Contract:	$2,804,271
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Effective Date of Contract:	30 March 1987
Contract Expiration Date:	28 February 1990
Contract No.:	N00014-87-C-0314
Program Manager:	W. R. Wisseman (214) 995-2451
Principal Investigator:	Frank Morris (214) 995-6392
Short Title of Work:	GaAs A-to-D Converter
Contract Period Covered by Report:	1 Oct. 1988 - 31 Dec. 1988

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St-A per telecon, Max Yoder, ONR/Code 1114SS.
Arl., VA 22217.

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I. SUMMARY

A. Brief Program Definition

This is a research and development program to design and fabricate both a GaAs high sampling rate A/D converter and a high resolution GaAs A/D converter.

B. ADC Development

The world's first functional 5-bit GaAs ADCs were fabricated during the past quarter. Fully functional 5-bit and 4-bit ADCs were fabricated along with fully functional sample-and-hold circuits on our most recent lot shipped to Hughes. The ADCs exhibited excellent linearity. Yields of the 5-bit and 4-bit ADCs were 16.7% and 15.3%, respectively. Sample-and-hold yields were as high as 92% for the best wafer.

The major factor leading to these good yields was a significant reduction in the emitter contact resistance. Typical emitter resistances for this lot were 15 to 20 Ω, whereas the emitter resistances on previous lots were typically greater than 50 Ω and frequently greater than 100 Ω. Significant progress has been made toward solving the contact resistance problem, as evidenced by these high yields as well as by in-process emitter resistance measurements made on ADC lots still in process and pilot lots designed to address this problem.

II. HETEROJUNCTION BIPOLAR PROCESS DEVELOPMENT

A. Baseline Process Development

The process development thrust during the past quarter has been toward reducing the contact resistivity for the emitter and collector contacts. The contact resistivity for the base contacts continues to be in the low 10^{-6} region and does not represent a problem. However, until recently the

contacts to the n-ohmic layers have been in the mid 10^{-5} to low 10^{-4} region and represented a serious obstacle to obtaining functional ADCs. Our previous standard n-ohmic contact metal was 500 Å Au/12%-Ge followed by 140 Å Ni, 800 Å TiN, 200 Å Ti, and 1000 Å Au. The TiN/Ti layer was applied to form a diffusion barrier between the thicker gold layer and the Au/Ge layer to prevent shorting of the base-emitter contacts by metal spikes, as described in previous reports.

In the old process the Au/12%-Ge was evaporated using commercially available premixed pellets from a resistance-heated boat. To ensure the Au/Ge mixture in the deposited film was the same as in the initial premixed pellet, no shutter was used between the GaAs wafers and the boat during the initial heating cycle. Our concern was that since each evaporated constituent has its own vapor pressure/temperature profile, the evaporated film would be different in composition from the starting pellets. We believed that if a shutter were used, the higher vapor-pressure material would be deposited on the shutter before the wafers were exposed, thus reducing the amount of that material available for deposition on the wafers. Various numbers and sizes of the Au/12%-Ge pellets were tested, but little or no correlation was found with the resulting contact resistivities.

In addition to evaluating the AuGe evaporation source, we also evaluated various plasma contact etches and preohmic metal clean-ups. Process lots were split: in some lots all the n-ohmic process was run in the DSEG pilot line, while in others some of the process was performed in the pilot line and some in the CRL development laboratory. In general, material run in the pilot line yielded lower contact resistivity.

While reviewing the data with the pilot line personnel, it became apparent that they were using a shutter during the initial stages of the Au/12%-Ge evaporation. The boat was then allowed to stabilize at the required evaporation temperature before the wafers were exposed to the metal flux. In addition, the pilot line personnel were using a lower deposition rate (5 Å/s vs 25 Å/s) than we. After duplicating their deposition conditions, we saw an immediate reduction in the n-ohmic contact resistivity. Figure 1 is a histogram showing typical results obtained with a GaAs pilot using the modified evaporation procedure. The median contact

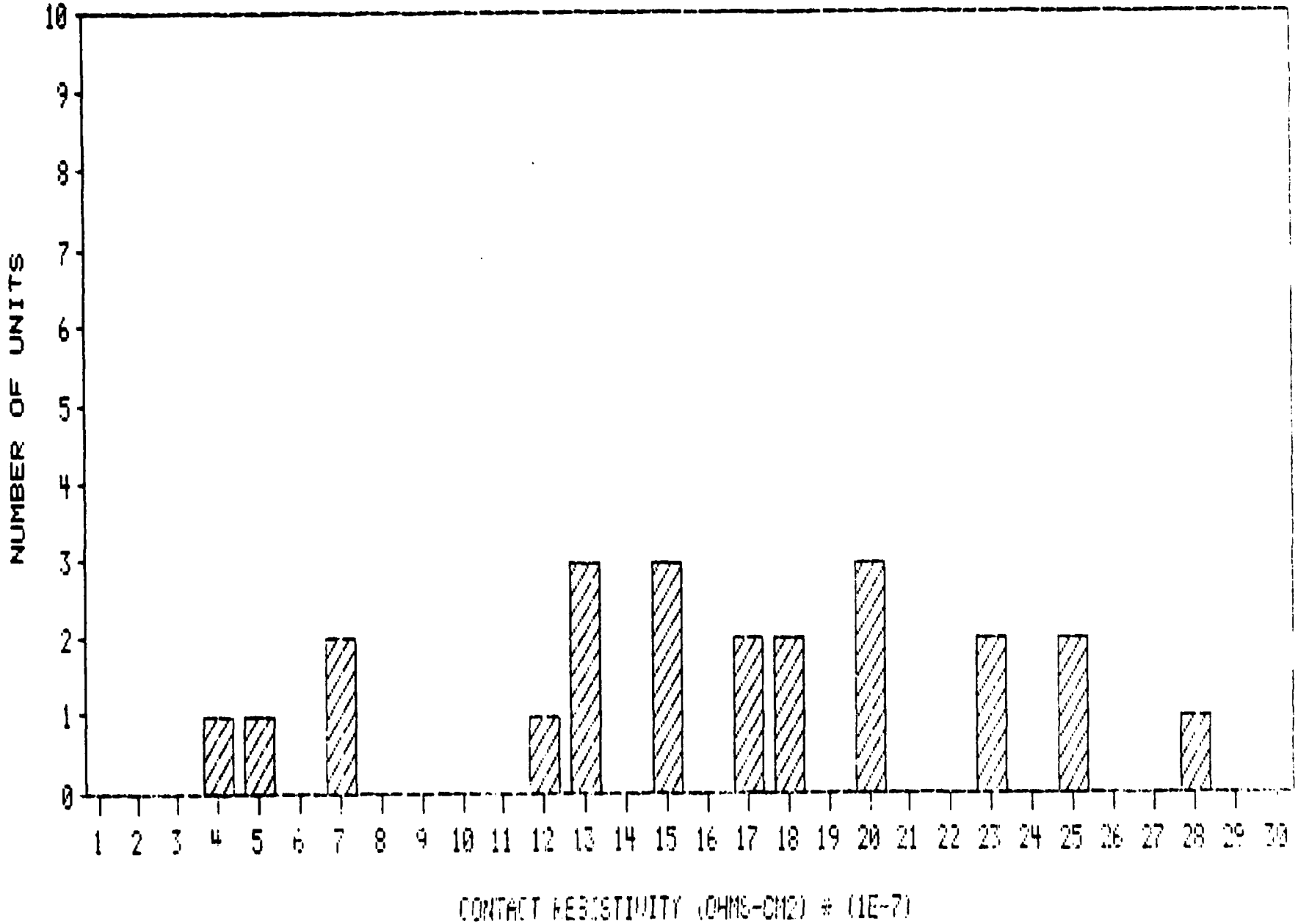


Figure 1. Contact resistivity for (Au/12%-Ge)/Ni/TiN/Ti/Au contacts.

resistivity is 1.4×10^{-6} Ω-cm^2, and the standard deviation is 7.3×10^{-7} Ω-cm^2. This process will be used on the ADC lots that are currently in the line. Hand-probing of ADC lots in process indicates that the emitter resistances on some of these wafers will be as low as those obtained on the high-yielding lot cited above. This process has become our new standard n-ohmic metal process and will be used for future ADC lots.

While this approach improves the contact resistivity, we found that the contact resistivity can still vary by an order of magnitude, depending on the thickness of the n^+ emitter cap layer. We believe this is due to the n-ohmic metal diffusing through the heavily doped GaAs cap layer to the more lightly doped GaAs cap layer during metal alloying; hence, the contact resistivity will be like that of a lightly doped semiconductor. Work is continuing to develop a suitable cap layer that has optimum thickness and doping to yield low contact resistivity and is also compatible with the n-channel JFET requirements.

In addition to the n-ohmic metal described above, other metal schemes are being evaluated to lower the contact resistivity further. Figure 2 shows the result of depositing 50 Å of Ni prior to depositing the Au/12%-Ge in the procedure described above. The Ni is believed to improve the wetting of the AuGe to the GaAs surface. For this wafer the median contact resistivity is 5×10^{-7} with a standard deviation of only 1.8×10^{-7}. This value is approximately one-third that obtained for the standard process described above, and this process resulted in a tighter distribution.

Another metal system that is being explored is Pd/Ge, which is believed to undergo a solid phase "regrowth" reaction with the GaAs, resulting in epitaxial Ge in contact with the GaAs surface. This process has the potential for further reducing the contact resistivity, as well as significantly lowering the incidence of metal spiking through the base-emitter junction. S. S. Lau, at UC-San Diego, has agreed to run some Pd/Ge evaporation and anneals for us. If these initial lot results are positive, we will pursue this approach more aggressively.

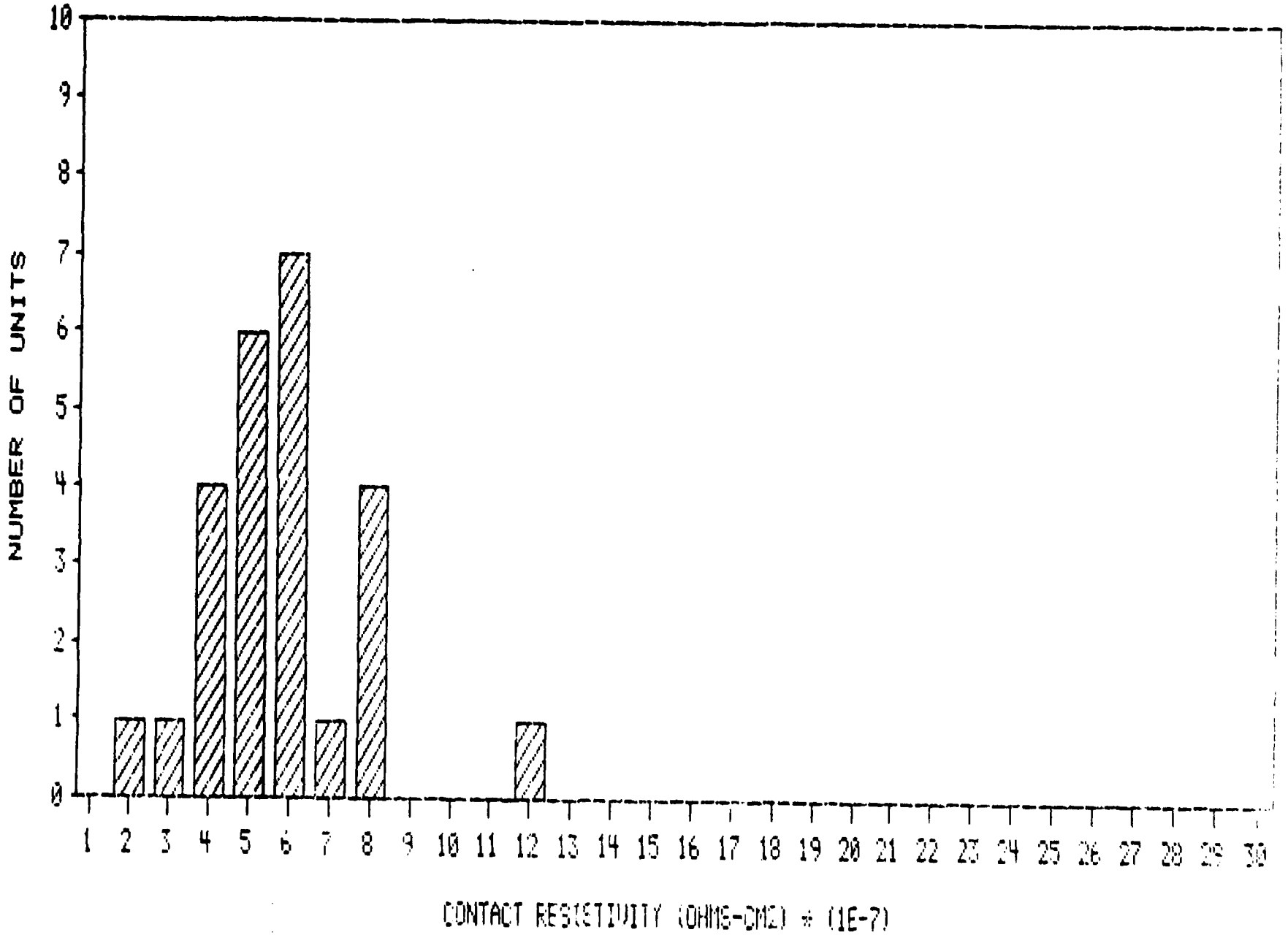


Figure 2. Contact resistivity for Ni/(Au/12%-Ge)/Ni/TiN/Ti/Au contacts.

B. Circuit Deisqn/Testing Progress

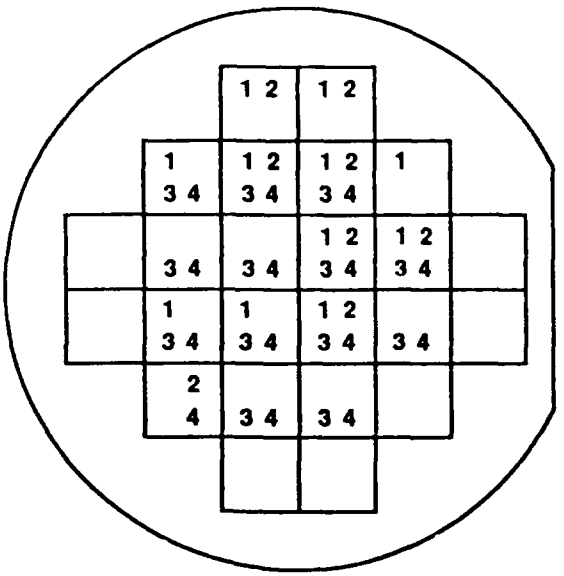
Two HBT lots (107 and 99) were received from Texas Instruments in mid-quarter and subsequently probed. Fully functional 5-bit and 4-bit ADCs were found on one of the two lots (107), thus verifying the designs. Wafer maps of the functional quantizers are shown in Figure 3. Yields of the 5-bit and 4-bit ADCs were 16.7% and 15.3%, respectively, and working ICs were located on both wafers.

A number of parameters were measured at wafer probe, including power supply currents, output voltage levels, and dc linearity. Most of the functional die exhibited supply currents and output voltage levels within 10% of expected design values, indicating good process uniformity. Figure 4 shows the results of dc linearity measurements on die-adjacent 5-bit and 4-bit ADCs. At probe, a sampling voltage tracker circuit was used to precisely determine the threshold of each comparator of the ADC under test. The resultant input voltage vs ADC output code transfer function is shown. The deviation between the ADC transfer function and a least-squares fit (LSF) line is also shown (residue). LSF linearity values for the 5-bit and 4-bit were 20 mV and 3.2 mV, respectively.

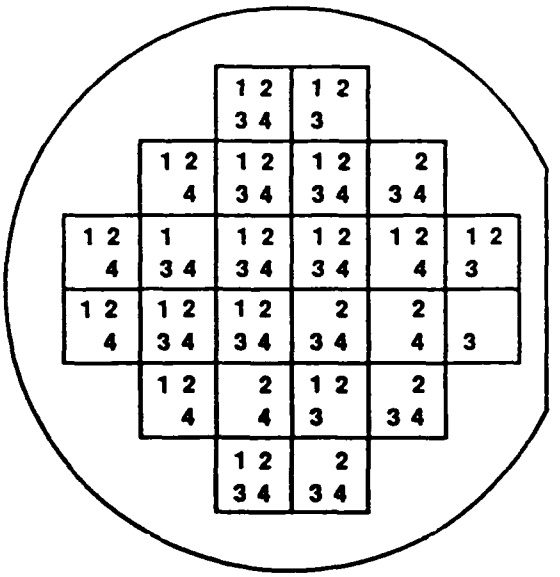
The excellent LSF linearity of the functional ADC indicates that differential pair V_{be} match has a 1 sigma variation <2 mV. Differential pair V_{be} measurements were nearly complete by the end of the quarter. A complete statistical V_{be} analysis will be available in January to provide both the V_{be} and current gain matching information required for the design of the 12-bit ADC.

Earlier in the quarter we initiated an effort to redesign the 5-bit and 4-bit ADCs to accept devices with high emitter resistances. However, since functional ADCs have been fabricated with Lot 107, the redesign effort has been terminated.

Wafer probing of the four sample-and-hold (S/H) circuits on Lots 107 and 99 was also completed this quarter. Wafer maps of the functional S/H on Lot 107 are shown in Figure 5. Functional yields for the four versions ranged from 33% to 92%; the average yield for each version across the lot was in



WAFER 107-C



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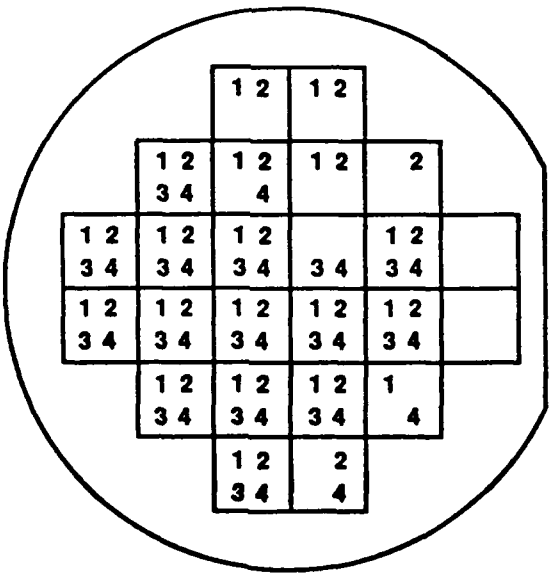


WAFER 107-E

Figure 3. Functional yield of 5-bit and 4-bit ADCs (HBT Lot 107, 11/88).

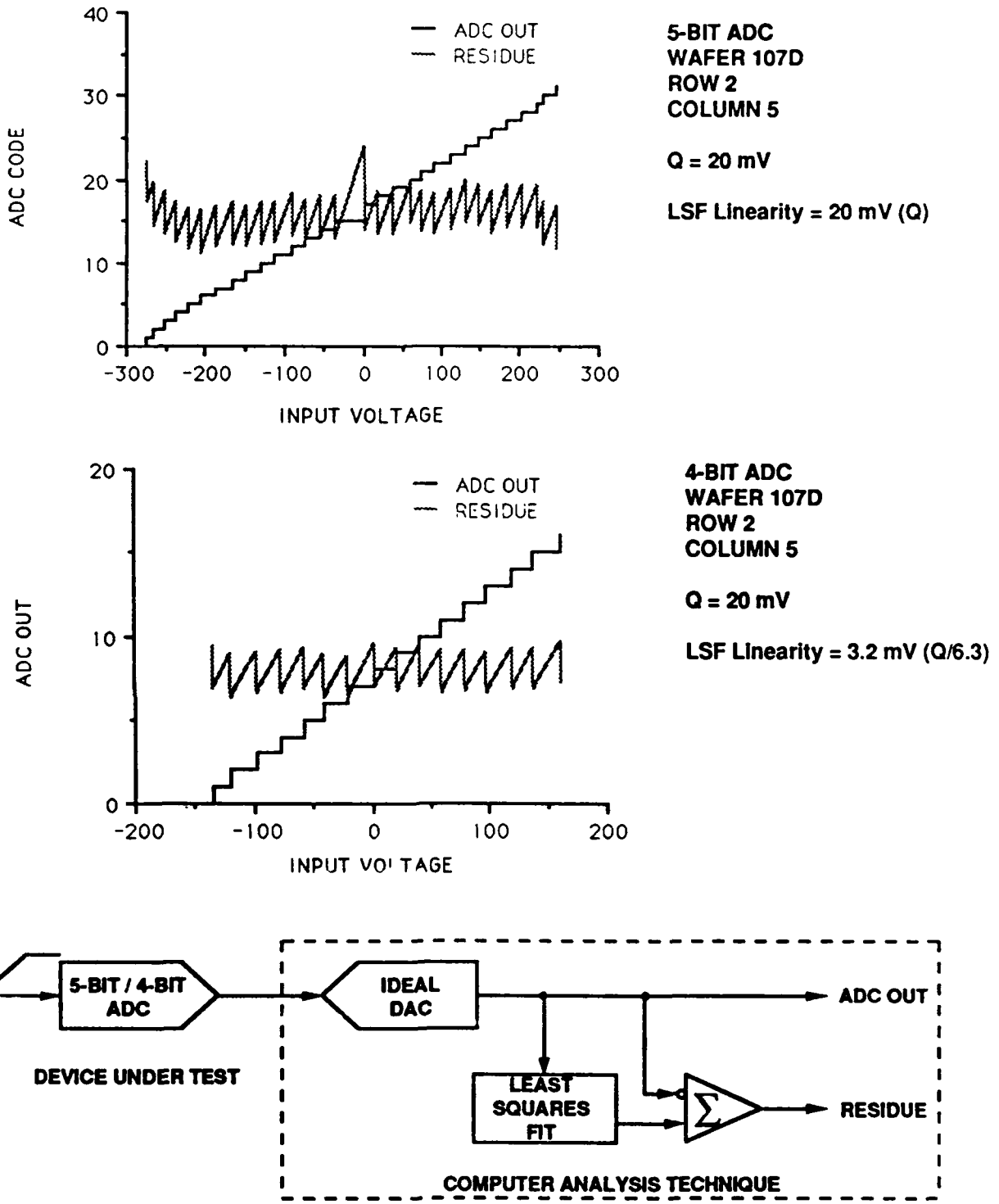


Figure 4. Measured least-squares fit linearity of die-adjacent 5-bit and 4-bit ADCs (Wafer 107D, 11/88).

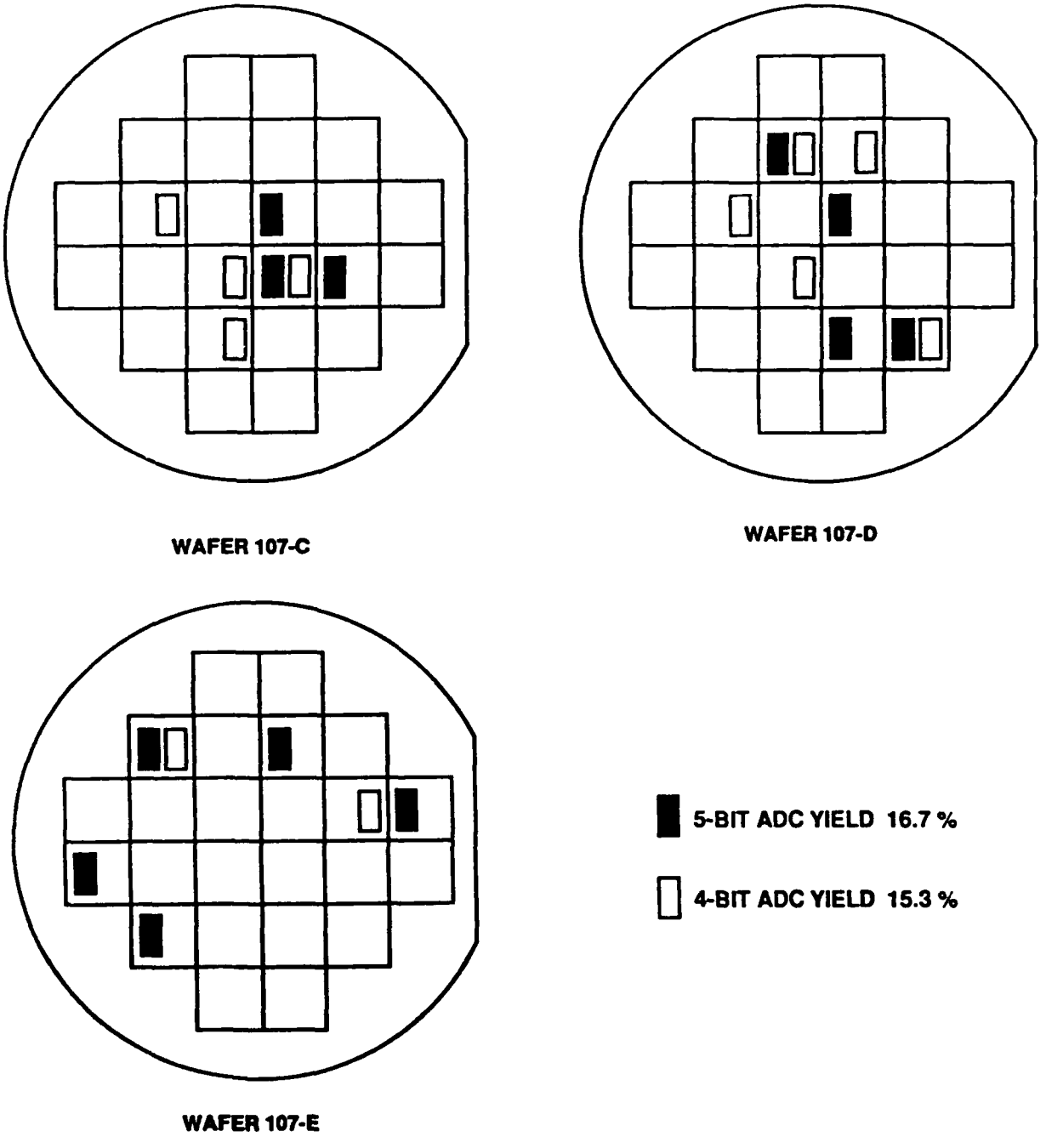


Figure 5. HBT S/H functional yield (four versions) from Lot 107, 11/88.

excess of 63%. Yield results are given in Table 1, and the differences between the four S/H versions are summarized in Table 2. S/H yields from Lot 99 (two wafers) varied from 8% to 63%; the average yield for all versions across the lot was 30%.

One of the three wafers from Lot 107 was returned to Texas Instruments for wafer saw. A representative sampling of functional 5-bit, 4-bit, and S/H die will be dynamically evaluated in January. All the fixturing required, including a custom thin-film test hybrid, is in place and ready for immediate testing of the HBT die. The measured dynamic performance of the HBT ADCs will serve to validate both our HBT device models and the folded circuit architecture employed in the 5-bit ADC.

The recent success of the 5-bit ADC design effort will now allow us to begin detailed design of the 12-bit ADC. A brief modeling effort, including HBT device noise analysis, will be performed in parallel with system-level circuit design in January.

Delays in the HBT process development, with the exception of the recent success of Lot 107, have resulted in significant slips in the release of both the 8-bit and 12-bit mask sets. As a result of the process problems and program delays, insufficient funding remains to complete the 8-bit and 12-bit A/D designs. Hughes is currently focusing its efforts on the 12-bit design and preparing an estimate to complete the 8-bit A/D. A mask set containing a complete 12-bit ADC is scheduled for release in July 1989.

C. Plans for Next Quarter

- Continue optimizing n-ohmic contact process.
- Optimize n-channel JFET process compatible with HBTs.
- Process 5-bit ADC lots.

Table 1
Sample-and-Hold (S/H) Yield Statistics From November Lot

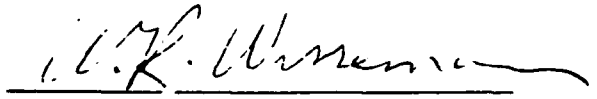
Wafer No.	S/H 1		S/H 2		S/H 3		S/H 4	
	Number Functional	Yield (%)	Number Functional	Yield (%)	Number Functional	Yield (%)	Number Functional	Yield (%)
107-C	11	46	8	33	13	54	14	58
107-D	17	71	22	92	17	71	20	83
107-E	19	79	20	83	15	63	18	75
Totals by S/H Version	47	65	50	69	45	63	52	72

Table 2
HBT Devices Used in Four Sample-and-Hold (S/H) Versions

Devices Used	S/H Versions			
	S/H 1	S/H 2	S/H 3	S/H 4
5 x 5 μm Bipolar Transistor	•		•	
7 x 7 μm Bipolar Transistor		•		•
5 x 5 μm Bipolar Diode	•			•
5 x 5 μm Schottky Diode		•		
3 x 3 μm Schottky Diode			•	

Note: Schottky diodes used in sampling gate only

- Complete differential pair V_{be} and β statistical matching analysis.
- Update HBT device models with measured data from Lot 107.
- Complete noise characterization of HBT devices.
- Begin dynamic characterization of 5-bit, 4-bit, and S/H circuits.
- Begin design of 12-bit ADC.



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